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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,464	01/15/2004	Chung-Ching Huang	TOP 350	5050

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EXAMINER	
BARTON, JONATHAN A	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,464	HUANG ET AL.	
	Examiner	Art Unit	
	Jonathan Barton	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claim 1 recites the limitations "the CPU" in lines 10-11, and "the memory cycle" in line 16. There is insufficient antecedent basis for these limitations in the claim.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 6, 7, 9-12, and 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shahar et al. (US 5,922,055) in view of Gulick et al. (US 2004/0250063).

a. As for claim 1 Shahar discloses

i. a storage device capable of storing a plurality of address records, each address record comprising an identity and an address range associated with a flash ROM (Col. 4 Lines 20-23);

ii. a strapping component, configured to output a signal to determine flash ROM type (Fig. 4 Item 8, Col. 5 Lines 23-30); and

iii. a process unit, coupled to the storage device and the strapping component (Col. 5 Lines 23-25),

iv. receiving a memory access request with an access range from the CPU and the signal (Col. 7 Lines 40-45),

v. determining the flash ROM type according to the signal (Col. 7 Lines 46-48),

vi. querying the identity by matching the access range and the address range (Col. 7 Lines 48-56).

b. Shahar fails to disclose the following limitation, which is taught by Gulick et al:

vii. executing an LPC 1.1 memory access instruction with the identity and the access range corresponding to the memory cycle (Par. 76 Lines 12-23).

viii. It would have been obvious to one of ordinary skill in the art to have combined the LPC 1.1 protocol taught by Gulick et al. with the ROM-type detecting system disclosed by Shahar et al. because the LPC 1.1 protocol was developed as a standard specification to make system interoperability and compatibility easier and more prominent, and thus it would make obvious sense to update the newest versions of Shahar's invention with this protocol.

c. As for claim 11 Shahar et al. disclose

ix. receiving a memory access request with an access range from a CPU (Col. 7 Lines 40-45);

x. receiving a signal output from a strapping component to determine flash ROM type (Col. 7 Lines 46-48);

xi. inputting a plurality of address records associated with a flash ROM, wherein the address record comprises an identity and an address range (Col. 7 Lines 52-56);

xii. querying the identity by matching the access range and the address range (Col. 7 Lines 48-56),

d. while Gulick et al. teach

xiii. executing an LPC 1.1 memory access instruction with the access range and identity corresponding to the memory cycle (Par. 76 Lines 12-23).

e. As for claim 2 and 14 Shahar et al. disclose

xiv. the identity is an "IDSEL" number associated with a firmware hub flash ROM (Col. 5 Lines 44-49).

f. As for claim 3 and 15 Shahar et al. disclose

xv. the address range is a pair comprising a base address and an end address (Col. 4 Lines 24-31).

g. As for claim 4 and 16 Gulick et al. teach

xvi. the address range is a pair comprising a base address and memory size (Par. 29).

h. As for claim 6 and 12 Shahar et al. disclose

xvii. the memory access request is a memory read request or a memory write request (Col. 3 Lines 43-45).

i. As for claim 7 and 17 Gulick et al. teach

xviii. in the process unit, the LPC 1.1 memory access instruction is an LPC memory read instruction or an LPC memory write instruction (Par. 84), and

xix. the LPC memory read instruction or the LPC memory write instruction corresponds to the LPC memory cycle (Par. 84).

j. As for claim 9 Gulick et al. teach

xx. a basic input/output system (BIOS) flag within the address record indicates whether the system BIOS is stored in flash ROM (Par. 87).

k. As for claim 10 Gulick et al. teach

xxi. a configuration unit detecting an error message indicating system BIOS failure, and resetting the BIOS flag for further reboot (Par. 92).

2. Claims 5, 8, 13, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shahar et al. (US 5,922,055) in view of Gulick et al. (US 2004/0250063) and further in view of Kao (US 6,745,329).

l. As for claim 5 and 13 Gulick et al. teaches

xxii. the flash ROM type is an LPC flash ROM (Par. 76 Lines 12-23).

m. The following limitation is not disclosed but is taught by Kao:

xxiii. a firmware hub flash ROM (Col. 1 Lines 21-26).

xxiv. It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined the firmware hub taught by Kao with the ROM identification system disclosed by the combination of Shahara and Gulick because both systems involve using ROMs for launching a BIOS and the firmware hub taught by Kao gives another commonly known within the art option for a type of ROM to use.

n. As for claim 8 and 18 Kao teaches

xxv. in the process unit, the LPC 1.1 memory access instruction is a firmware hub memory read instruction or a firmware hub memory write instruction (Col. 1 Lines 21-26), and

xxvi. the firmware hub memory read instruction or the firmware hub memory write instruction corresponds to the firmware hub memory cycle (Col. 1 Lines 21-26).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan Barton whose telephone number is 571-272-8157. The examiner can normally be reached on Monday - Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jonathan Barton
Examiner
Art Unit 2186

JB

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100